In re Patent Application of:
FRANCIS ET AL.
Serial No. **10/008,586**
Filing Date: **NOVEMBER 5, 2001**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The arguments supporting patentability of the claimed invention are presented below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 12, 20, 26 and 31 over the Smith patent in view of the Matoba patent. The present invention, as recited in independent Claim 12, for example, is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each responsive to a respective local clock signal, and at least one system clock connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals. A power control manager is connected to the circuit blocks via respective clock enable lines for selectively providing a shutdown signal thereto. The power control manager comprises at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals. Each circuit block comprises a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

An advantage of the present invention is that the shutdown circuit in each circuit block allows the circuit block to be safely shutdown after receiving the shutdown signal. It can be difficult to establish an exact time when it is possible to switch off the clock to a circuit block

without causing errors. By storing the logic state of the shutdown signals in the at least one register, a determination can be made whether the circuit blocks are receiving the system clock signal, or the circuit blocks are in the shutdown state or completing its necessary operations before shutting down.

Independent Claim 20 is similar to independent Claim 12 except this claim recites a clock signal instead of a local clock signal, and each circuit block further comprises a block logic circuit providing a status signal indicating whether the circuit block is in an active or idle state. Independent method Claim 31 is similar to independent device Claim 12.

Independent Claim 26 is similar to independent Claim 12 except this claim recites a clock signal instead of a local clock signal, and further recites a central processing unit connected to the power control manager for determining whether each circuit block is in an active or idle state by querying the at least one register.

Referring now to Smith and to FIG. 1 in particular, the Examiner characterized the illustrated integrated circuit as a system-on-chip (SOC) comprising a plurality of circuit blocks **11-14**, a system clock connected to the circuit blocks for providing a system clock signal **35** thereto, and a power control manager **1** connected to the circuit blocks for selectively providing a shutdown signal **15-18** thereto. The Examiner characterized each circuit block **11-14** as comprising a shutdown circuit (NAND gates **27-30** and **44-47**, flip-flops **23-26** and inverters **36-39**) for preventing the system clock signal **35** from functioning as the respective local clock signal based upon the shutdown signal.

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The Examiner correctly acknowledges that Smith fails to disclose at least one register in the power control manager **1** for storing data indicating logic states of the shutdown signals for the current blocks **11-14**. The Examiner cited Matoba as disclosing this feature. FIG. 1 of Matoba discloses a power control manager **15** comprising a register **16a** connected to respective clock enable lines **INTR0-INTR3** for storing data indicating logic states of the shutdown signals.

The Examiner maintains his position that since Smith discloses a power control manager **1** connected to the circuit blocks **11-14** for selectively providing a shutdown signal **15-18** thereto, it would have been obvious to modify the power control manager **1** based upon Matoba to include at least one register for storing data indicating logic states of the shutdown signals. The Examiner goes on to further state that one of ordinary skill in the art would have been motivated to make such a combination because it "provides a way for controlling power consumption amongst multiple functional blocks though various detecting means."

As the Examiner is aware, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Since Smith is already directed to reducing power consumption in electronic devices, there is no motivation to include a register in the power control manager **1** of Smith for storing data indicating logic states of the shutdown signals. Reference is directed to column 1, lines 10-14 of Smith, which provides:

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> "More particularly, the invention preferably relates to an integrated design which conserves power by gating the generation of the clock signal individually to its multiple sub-circuits when they do not require a clock signal." (Emphasis added.)

In fact, Smith teaches away from using a register in the power control manager **1** because the power control manager **1** operates in response to the addresses received on the system bus **9**. The addresses themselves determine whether the circuit blocks **11-14** are to be powered on or shutdown. Reference is directed to column 2, lines 53-67 of Smith, which provides:

> "The central arbiter **1** and the comparison circuitry **2** monitor the system bus **9** for addresses within the range controlled by the central arbiter **1** and for specific corresponding commands, whose completion will require the operation of this electronic system or integrated circuit. When an address within the controlled range and a specific corresponding command is detected, the central arbiter **1** then determines which functional blocks **11-14** will be necessary for completion of its task. Once the central arbiter **1** determines which functional blocks **11-14** will be required for operation, the central arbiter **1** pulls the respective Start_Clock signal lines **15-18** to a logical low voltage level, causing the output of the respective NAND gates **44-47** to switch from a logical low voltage level to a logical high voltage level." (Emphasis added.)

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Reference is also directed to column 3, lines 13-20 of Smith, which provides:

> "The system bus **9** is coupled as an input to the central arbiter **1**. The central arbiter **1** is coupled to the comparison circuitry **2** through the address lines **7** which provide the address from the system bus **9** to the comparison circuitry **2**. The comparison circuitry **2** is also coupled to the central arbiter **1** through the control line **8** which informs the central arbiter **1** when the address on the address lines **7** is in the range of addresses controlled by the central arbiter **1**." (Emphasis added.)

When an address received by the system bus **9** is within a range of an address controlled by the power control manager **1**, then the power control manager **1** will provide a shutdown signal to the circuit blocks **11-14**. Instead of storing the logic states of the shutdown signals in the power control manager **1**, the power control manager **1** continuously monitors the system bus **9**. (Column 7, lines 10-14 of Smith.) Upon detecting that the system needs to transmit or receive signals, the power control manager **1** re-enables the clock signal to the circuit blocks **11-14** which are required for the transmission or reception.

There is no need for a register in the power control manager **1** since the device providing the addresses has already made a determination as to whether or not the circuit blocks **11-14** are to be in an active state. The comparison circuitry **2** simply makes a comparison of the received address and operates in response to it by gating the generation of the clock signal individually to its multiple sub-circuits when

they do not require power. Smith thus fails to make any reference to the logic states of the respective clock enable signals being stored in the power control manager 1.

Applicants thus assert that only in hindsight, and having the benefit of the Applicants' disclosure, would the skilled artisan possibly be motivated to modify the power control manager 1 in Smith to include a register as disclosed in Matoba. In other words, one skill in the art would not look to modify Smith absent having the benefit of studying the Applicants' disclosure.

Therefore, the Applicants submit that independent Claim 12 is patentable over Smith in view of Matoba. Independent Claims 20 and 31 and independent Claim 26 are similar to independent Claim 12, and it is submitted that these claims are also patentable over Smith in view of Matoba. In view of the patentability of independent Claims 12, 20, 26 and 31, their respective dependent claims, which recite yet further distinguishing features, are also patentable, and require no further discussion herein.

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CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 25 day of April, 2005.